Patent
Attorney's Docket No. 032326-073

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Pascal COOREMAN et al	)	Group Art Unit: 2876
	)	
Application No.: 09/601,111	)	Examiner: Ahshik Kim
	)	
Filed: July 27, 2000	)	Appeal No.
	)	
For: MICROPROCESSOR CARD INCLUDING A CABLE COMMUNICATION CIRCUIT	)	

BRIEF FOR APPELLANT

Mail Stop APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This appeal is from the decision of the Primary Examiner dated February 26, 2003, finally rejecting claims 1 and 6-8, which are reproduced as an Appendix to this brief.

A check covering the [ ] $165.00 (2402) [X] $330.00 (1402) Government fee and two extra copies of this brief are being filed herewith.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. A copy of this page and the signature page are submitted in duplicate.

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I. Real Party in Interest

The assignee of the present application is Gemplus, a French corporation, as recorded in the records of the Patent and Trademark Office at Reel 011010, Frame 0552.

II. Related Appeals and Interferences

There are no other appeals or interferences known to the Appellants, their legal representative, or the assignee which will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. Status of Claims

The present application contains eight claims. Claims 2-5 have been identified as containing allowable subject matter. Claims 1 and 6-8 stand finally rejected, and are the subject of this appeal.

IV. Status of Amendments

No amendments were filed subsequent to the final Office Action.

V. Summary of the Invention

The claimed invention relates to microprocessor cards, commonly known as "smart cards." The basic structure of a smart card is illustrated in Figure 1 of the application. The card 30 contains a microprocessor 10 that includes a central processing unit 12, a program memory 16, a data memory 18, and a working memory 14, e.g. a random access memory. To perform a transaction with the card, it is typically inserted into a terminal 20. The microprocessor 10 on the card communicates with the terminal 20 by means of a set of contacts 22.

Conventionally, the microprocessor was directly linked to the contacts 22, as represented by the dashed arrow 32. In this type of arrangement, electrical signals received from the terminal 20 were analyzed within the microprocessor, in accordance with

a dedicated communication program stored in the program memory 16. The analysis of the signals occupied significant resources of the central processing unit 12. In addition, the storage of the communication program and the data associated with the analysis consumed a considerable portion of the various memories (page 1, line 8 to page 2, line 7).

The objective of the claimed invention is to relieve the microprocessor of the tasks associated with analysis of the communications between the card and the terminal. Due to the limited amount of memory that is available in a smart card, the invention also seeks to free up memory for other purposes. In accordance with the invention, these objectives are achieved by providing a hard-wired communication circuit 40 between the microprocessor 10 and the contacts 22. The communication circuit includes a pulse generator, or pulse shaping circuit 34, that analyzes the electrical signals received from the terminal 20 and presents binary pulses to the remaining components of the communication device (page 4, line 27 to page 5, line 3). These binary pulses are supplied to an error checking circuit 36, which determines the integrity of the signals received from the terminal 20. The integrity check is performed, for example, by examining a parity bit or an error checking code, such as a redundant cyclic code, in the received signal. The error checking circuit 36 generates a signal on line 50 that indicates the results of the integrity check. This signal is supplied to a transmission circuit 48, which provides it to the terminal 20 by means of the contacts 22 (page 5, lines 4-12; page 6, lines 6-10 and 19-30).

In addition to checking the integrity of signals received from the terminal, the communication device 40 also includes a decoder 38 for determining the characters of commands, addresses and data in the received signal, and registers 42, 44 for storing this information. An acknowledgment circuit 52 provides a signal on a link 54 which indicates whether a command has been correctly received. This signal is also returned to the terminal 20, by means of the transmission circuit 48. Communications from the microprocessor 10 to the terminal are stored in a register 46, and then forwarded to the terminal by means of the transmission circuit 48 (page 5, line 13 to page 6, line 5).

VI. The Issues

The final Office Action presents a single issue for review, namely whether claims 1 and 6-8 are unpatentable under 35 U.S.C. §103, when the Kim et al patent (U.S. Patent No. 5,729,004) is considered in view of the Anderl et al patent (U.S. Patent No. 4,816,654).

VII. Grouping of Claims

Appellants do not consider all finally rejected claims to stand or fall together. Specifically, even if claim 1 should be found to be unpatentable over the applied references, separate grounds of patentability exist with respect to claim 8. Arguments for the separate patentability of claim 8 are presented hereinafter.

VIII. Argument

A. *Claim 1*

Claims 1 and 6-8 stand finally rejected under 35 U.S.C. §103, as being unpatentable over the Kim et al patent in view of the Anderl et al patent. The Kim et al patent is directed to smart cards. In Figures 1 and 2, it discloses that a smart card has an I/O circuit 11, 21 disposed between the card's CPU and its contacts. The basic structure of the I/O circuit is illustrated in Figure 3. This circuit includes, among other components, a parity detector 35. An exclusive NOR gate 37 compares a parity bit RPB that is received from the terminal with an operation parity bit DPB that is computed in a parity operator 34, on the basis of data received from the terminal. If these two bits match, a NOR gate 38 of the parity detector 35 outputs a parity detection signal PBT at a logic low level, indicating that the data was properly received. On the other hand, if the received parity bit RPB and the operation parity bit DPB do not match, the NOR gate 38 outputs a high level signal, to indicate that the received data is in error. (See column 5, lines 8-21.)

At column 10, lines 19-22, the Kim et al patent states that "the controller of the smart card device analyzes the logic of the parity detection signal PBT...." The purpose of

this analysis is to enable the controller, i.e. the card's CPU, to determine whether to load data received from the terminal and stored in a data register 32 of the I/O device.

Claim 1 recites a card having a microprocessor and contacts via which the card communicates with a terminal. The claim further recites a communication device in the form of a hard-wired circuit disposed between the contacts and the microprocessor. This communication device operates according to an asynchronous communication protocol, to check the integrity of signals transmitted between the microprocessor and the terminal. The claim recites that the communication device "includes means to generate and return at least one item of information to the terminal which is a function of the signals received."

The final Office Action acknowledges that the data communication device disclosed in the Kim et al patent, namely the I/O device 30, does not return at least one item of information to the terminal, which is a function of signals received. To this end, therefore, the rejection relies upon the Anderl et al patent. With particular reference to column 10, lines 38-46 and column 11, lines 36-53, the Office Action states that this patent discloses a memory card 10 that resends data to a terminal after an initial attempt to send data to a reader 15 results in the reader transmitting an "error-in-data-integrity" signal or "unsuccessful-data-transmittance" signal. Based upon this teaching, the Office Action alleges that it would have been obvious to design the card of the Kim et al patent to respond to an integrity signal transmitted by the terminal.

Even if this general conclusion of obviousness is accepted, it does not lead a person of ordinary skill in the art to the subject matter recited in claim 1. The Kim et al patent teaches that the parity detection signal PBT is provided to the card's CPU. Utilizing the teachings of the Anderl patent in this context, therefore, would result in the generation of an acknowledgment signal by the CPU, which could then be presumably passed back to the terminal via the I/O device 30. Such an arrangement is not the same as the claimed subject matter, however. As described in the specification and the summary section of this Brief, the function of the communication device of the present invention is to relieve the microprocessor of the duties normally associated with analysis of the signals received from

the terminal, as well as free up memory that stores the program for conducting such analysis. Such a result is not accomplished by the combination of teachings proposed in the final Office Action. While the I/O device may function to pass response signals back to the terminal, the analysis of the received signals and the generation of those responses is still carried out within the card's *microprocessor*, rather than the I/O device. In other words, in the proposed combination of references, the intelligence for determining whether to return information to the terminal, as a function of the received signals, resides within the card's CPU. In contrast, in the present invention, that function is performed within the communication device itself, so that the card microprocessor is free to perform other tasks.

With reference to the language of the claims, there is no disclosure in the Kim et al patent that the I/O device 30 functions to "*generate and return* at least one item of information to the terminal which is a function of the signals received." Rather, in that device the only information which is generated as a function of the signals received, namely the signal PBT, is sent on to the card's CPU, rather than returned to the terminal. The Anderl et al patent does not contain any disclosure which would lead one of ordinary skill in the art to modify this type of operation. Specifically, there is no disclosure that information is generated as a function of signals received from the reader 15, and returned to the reader, by the card's interface circuit 130.

Since neither of the references teaches a card having a communication device of the type recited in claim 1, whether considered individually or in combination, the Office Action has failed to make out a prima facie case of obviousness.

B. *Claim 8*

Furthermore, even if claim 1 is not considered to be patentable over the teachings of the Kim et al and Anderl et al patents, claim 8 recites additional subject matter that supports separate patentability of this claim. Specifically, this claim recites that an item of information generated by the communication device comprises an indication whether a *command* contained in a signal received from the terminal is complete and correct. With reference to the disclosed embodiment, for example, a decoder 38 determines each

character of a received command, and an acknowledgment circuit 52 generates a signal on link 54 which indicates whether the received command is complete and correct.

There is no disclosure in the Kim et al patent suggesting that the I/O device 30 analyzes *commands* in such a fashion. Rather, the parity detector 35 only determines whether the parity of a received *byte* is correct. There is no attempt to determine whether a received byte pertains to a command, and if so whether that command is complete and correct.

While the Anderl et al patent discloses the generation of ACK and NAK responses to messages received from a station 18 (see column 11, lines 36+), there is no suggestion that these responses are generated in the card's interface circuit 130. To the contrary, since an ACK response indicates that a *transaction* has been successfully completed, the obvious implication is that this signal is generated by the microprocessor, which performs the transaction, rather than the interface circuit which is merely disclosed as "coupling" data between the reader 15 and the card's microprocessor 110 (column 4, lines 31-37).

For these additional reasons, therefore, the Office Action has not set forth a prima facie case to support the rejection of claim 8. In fact, it is to be noted that the final Office Action does not even address the particular subject matter of this claim.

IX. Conclusion

The references applied in the final rejection of the claims, when considered either individually or in combination, do not suggest a hard-wired communication device that is disposed between the microprocessor and the contacts of a smart card, and that generates and returns an item of information to the terminal which is a function of signals received

from the terminal. Only Appellants' specification discloses a smart card having such features. The rejection of the claims is not properly founded in the statute, and should be reversed.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
James A. LaBarre
Registration No. 28,632

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

Date: November 28, 2003

APPENDIX A

The Appealed Claims

1. A card with a microprocessor and contacts, and a communication device in the form of a hard-wired circuit disposed between the contacts and the microprocessor and operating according to an asynchronous communication protocol to check the integrity of signals transmitted between the microprocessor and a terminal, wherein said communication device includes means to generate and return at least one item of information to the terminal which is a function of the signals received.

6. The card of claim 1, wherein the item of information generated by said generating means comprises an indication whether a signal received from the terminal contains an error.

7. The card of claim 6, wherein said generating means generates said indication on the basis of redundant information contained in the received signal.

8. The card of claim 1, wherein the item of information generated by said generating means comprises an indication whether a command contained in a signal received from the terminal is complete and correct.

the terminal, as well as free up memory that stores the program for conducting such analysis. Such a result is not accomplished by the combination of teachings proposed in the final Office Action. While the I/O device may function to pass response signals back to the terminal, the analysis of the received signals and the generation of those responses is still carried out within the card's *microprocessor*, rather than the I/O device. In other words, in the proposed combination of references, the intelligence for determining whether to return information to the terminal, as a function of the received signals, resides within the card's CPU. In contrast, in the present invention, that function is performed within the communication device itself, so that the card microprocessor is free to perform other tasks.

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